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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/942,962	08/31/2001	Takaaki Sasaki	TAI 131	7694

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EXAMINER
ZARNEKE, DAVID A

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 11/05/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/942,962	SASAKI, TAKAAKI	
	Examiner	Art Unit	
	David A. Zarneke	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 August 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13 and 24-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13, 24-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 8/22/2 have been fully considered but they are not persuasive. Applicant makes one main argument, that being that Yamashita fails to teach the electrodes being level with the upper surface of the sealing resin.

The examiner asserts that Yamashita, in Figure 3, does indeed teach this limitation. See the *35 USC § 102* rejection below for details.

Also, applicant added 3 new claims, 2 of which are independent claims. These independent claims add a wiring pattern attached to the top surface of the sealing resin.

The examiner takes the position that the combination of Yamashita and Aiba teaches this limitation, as detailed in the previous office action. See the *35 USC § 103* rejection below for details.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 7, 8, 11 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamashita et al., US Patent 5,726,493.

Yamashita teaches a semiconductor package (Figure 3) comprising:

a printed circuit base (11) having a prescribed electrode pattern on each side thereof and electrically connected together by through holes (15);

a semiconductor chip (12) placed upon the upper surface of the PCB (11) and electrically connected to the upper electrode pattern using bond wires (14);

a sealing resin (16) which seals the semiconductor chip (12) and the upper electrode pattern;

a plurality of electrode members (22) formed in the sealing resin (16), one end of which is electrically connected to the through holes (23) of the upper electrode pattern (15) and the other is level with the top of the sealing resin (16); and

a plurality of pads (13) formed on the lower electrode pattern for solder ball (13) placement.

Regarding claim 2, Yamashita teaches a plurality of solder balls (13) formed on the lower surface (11b) of the PCB (11) (Figure 1) and alternatively, a plurality of solder balls (13) formed on the end of the electrode members (17) (Figure 11).

With respect to claim 3, Yamashita teaches attaching a second PCB (11) to the surface of the sealing resin (16), the second PCB (11) having an electrode on each side thereof, the lower electrode pattern electrically connected to the electrode members, and the upper electrode pattern electrically connected to the lower electrode pattern by through holes (15), wherein a 2nd electrode is formed in the second PCB at the surface of the sealing resin where the electrode members are exposed (Figure 11).

As to claim 4, Yamashita teaches solder balls (13) connecting the electrode members (17) of the first PCB to the lower electrode pattern of the 2nd PCB (Figure 11).

Regarding claim 7, Yamashita teaches the 1st and 2nd electrodes to be disposed at different positions in horizontal directions (Figure 11).

With respect to claim 8, Yamashita teaches a 2nd semiconductor chip (12) placed upon the upper surface of the 2nd PCB possibly having a different function (Figure 11).

As to claims 11, Yamashita teaches mounting the package upon a motherboard (18) (Figure 2).

Regarding claim 12, Yamashita teaches stacking the packages in various ways and using various techniques (Figures 11-16).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5, 6, 9, 10 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita et al., US Patent 5,726,493, as applied to claim 1 above, and further in view of Aiba et al., US Patent 6,348,728.

Regarding claims 5 and 6, Aiba teaches semiconductor device comprising a redistribution layer formed upon the surface of a sealing resin covering a chip, wherein a metal pattern (18a) is coated over a sealing resin (28), an insulating resin covers the metal pattern and lands (18b) [3rd electrode], which are electrically connected to the metal pattern (18a), are exposed there through (Figure 5B & 7, 51+).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the redistribution layer of Aiba in the invention of Yamashita because

redistribution layers are conventionally known in the art and the use of conventional materials to perform there known functions in a conventional process is obvious. In re Raner 134 USPQ 343 (CCPA 1962). Redistribution layers are commonly known in the art and are used to increase the mounting area of a semiconductor device to enable mounting to proceed using conventional techniques (Aiba, 1,66+).

With respect to claim 9, Yamashita and Aiba combined teach the 1st and 3rd electrode to be disposed at different positions in horizontal directions.

As to claim 10, Yamashita teaches the electrically connecting of more than 1 chip onto the upper surface of the 2nd printed circuit base, possibly having a different function than the other chips (Figure 16).

Regarding claim 13, Aiba teaches the use of memory elements in amongst the chips to be packaged (Figure 1A-1D).

Claims 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita et al., US Patent 5,726,493, in view of Aiba et al., US Patent 6,348,728.

Yamashita, relied upon as recited above, fails to teach a wiring pattern being added to the top of the sealing resin.

Aiba teaches semiconductor device comprising a redistribution layer formed upon the surface of a sealing resin covering a chip, wherein first wirings (18a) and second wirings (18b) are coated over a sealing resin (28), an insulating resin covers the wirings and then the second wirings, which is electrically connected to the first wirings, are exposed there through (Figure 5B & 7, 51+), and wherein one wiring is closer to the center of the package and the other is closer to the periphery of the package.

As to claim 25, Aiba teaches the a plurality of 1st and 2nd wirings that are alternatingly arranged (Figure 5B).

Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita et al., US Patent 5,726,493, in view of Aiba et al., US Patent 6,348,728.

Yamashita, relied upon as taught in the rejection of claims 24 and 25, fails to teach a wiring pattern formed on the sealing resin and electrically connected being made of Cu and an electrode formed on the wiring pattern and being made of a Ni layer and a Au layer.

Aiba, relied upon as taught in the above rejection of claims 24 and 25, teaches forming a wiring pattern (18 and 34) upon the surface of the sealing resin having Cu (7, 58+) posts (32) and an solder ball electrode (36) formed thereon (Figure 7B).

Regarding the use of a Ni layer under a Au bump, the examiner takes "official notice" since the claimed subject matter is notoriously well-known in the art (MPEP 2144.03). The formation of a Ni layer under a Au bump is commonly used in the art to prevent interdiffusion of a Cu wiring and an Au bump.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David A. Zarneke whose telephone number is (703)-305-3926. The examiner can normally be reached on M-F 10AM-6PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on (703)-305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703)-308-7722 for regular communications and (703)-308-7721 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-308-0956.

David A. Zarneke
October 28, 2002

ALBERT W. PALADINI
PRIMARY EXAMINER